INFORMATION DISCLOSURE CITATION *(USE SEVERAL SHEETS IF NECESSARY)*	ATTY DOCKET NO. DE920000008US1	SERIAL NO. 09/838,068
	APPLICANT(S) HALLER ET AL.	
	FILING DATE 04/19/2001	GROUP ~~2126~~ 2154

OIPE JC
FEB 2 6 2004
PATENT & TRADEMARK OFFICE

RECEIVED
MAR 0 3 2004
Technology Center 2100

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
M.P.	AA	5,740,393	04/14/1998	Vidwans et al.	395	391	
	AB	5,627,984	05/06/1997	Gupta et al.	395	392	
	AC	5,584,038	12/10/1996	Papworth et al.	395	800	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION		
							NO	YES	ABSTRACT

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AD	Farrell, et al., "Issue Logic for a 600-MHz Out-of-Order Execution Microprocessor," IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998, pp. 707-712.
MP	AE	Palacharla, et al., "Complexity-Effective Superscalar Processors," ISCA '97 Denver, CO, USA, 1997 ACM 0-89791-901-7/97/0006, pp. 206-218.
	AF	Gaddis, et al., "A 56-Entry Instruction Reorder Buffer," ISSCC96/Session 13/Microprocessors/Paper FP 13.2, 1996 IEEE International Solid-State Circuits Conference, pp. 212-213, 447.

EXAMINER	**DATE CONSIDERED** 5/11/04

EXAMINER: Initial here if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. **Include copy of this form with next communication to applicant.**